CHI MEI OPTOELECTRONICS CORP.

Issue Date:Jul.23.2009
Model No.: V470H2-LH2
Approval

TFT LCD Approval Specification

MODEL NO.: V470H2 – LH2

Customer: _____

Approved by:_____

Note:

Approved By	TV Product Marketing & Management Div
	Chao-Chun Chung

Reviewed By	QA Dept.	Product Development Div.
	Hsin-nan Chen	WT Lin

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver. 2.0	Apr. 01. 2009	All	All	The approval specification was first issued.
Ver. 2.1	Apr. 27 2009	7	2.1	ABSOLUTE RATINGS OF ENVIRENMENT
		13	3.2.3	INVERTER INTERFACE CHARACTERISTICS
		15	4.1	TFT LCD MODULE
Ver. 2.2	Jul. 01, 2009	1	Cover	Modify the owner of QA Dept. and LCD TV Marketing and Product Management Div.
		5	1.4	Modify the Pixel Pitch
		37~39	Chapter11	Modify the enhanced ribs of Metal Frame Rear drawing.
		36	10.1	Modify Box dimensions
Ver. 2.3	Jul. 23, 2009	37~39	Chapter11	Add a rectangular hole on ribs of Metal Frame Rear drawing.
		1	Cover	Modify the Approved dept. and owner as TV Product Marketing & Management Div and . Chao-Chun Chung.
		6	1.4	Modify the Depth of module size
		29	7.2	Add the Typ. and Max. value of response time

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V470H2-LH2 is a 47" TFT Liquid Crystal Display module with 12-CCFL Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display true 1.07G colors (10-bit/color). The inverter module for backlight is built-in.

1.2 FEATURES

- High brightness (500 nits)
- High contrast ratio (4000:1)
- Fast response time (Gray to gray average 4.0 ms)
- High color saturation (NTSC 72%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 120 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- RoHS compliance

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1039.68 (H) x584.82 (V) (47" diagonal)	mm	(1)
Bezel Opening Area	1049(H) x 539 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.5405 (V) x 0.1805 (H)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.07G	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (Haze 11%)/ Hard coating (3H)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec. of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATION

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	-	1096	-	mm	(1), (2)
	Vertical (V)	-	640	-	mm	
	Depth (D)	-	48.5	-	mm	
Weight		-	12500	-	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth is between bezel to T-CON cover.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol		Value		Unit	Note
			Min.	Max.		
Storage Temperature	TST		-20	+60	ºC	(1)
Operating Ambient Temperature	TOP		0	50	ºC	(1), (2)
Shock (Non-Operating)	SNOP	X,Y axis	-	50	G	(3), (5)
		Z axis		35	G	(3), (5)
Vibration (Non-Operating)	VNOP		-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

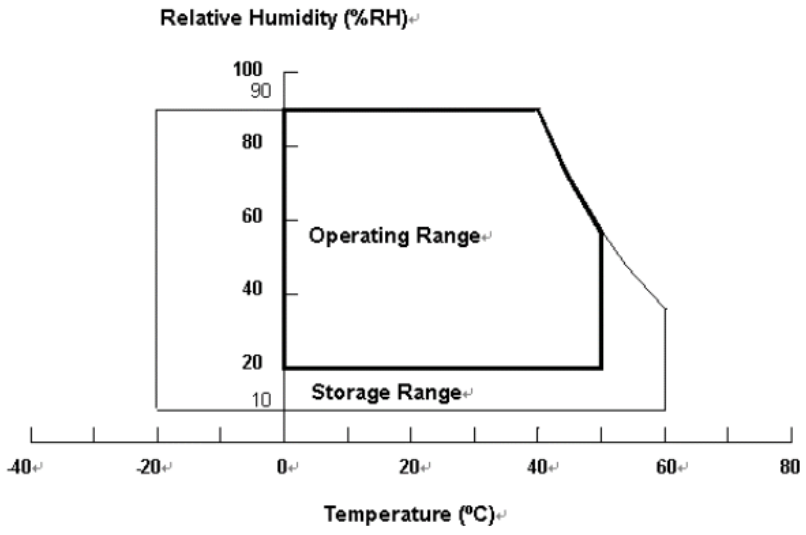
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stroed in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

2.3.2 BACKLIGHT INVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	VW	—	3000	VRMS	
Power Supply Voltage	VBL	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Contro.l Internal PWM Control and External PWM Control.

3. ELECTRICAL CHARACTERISTICS

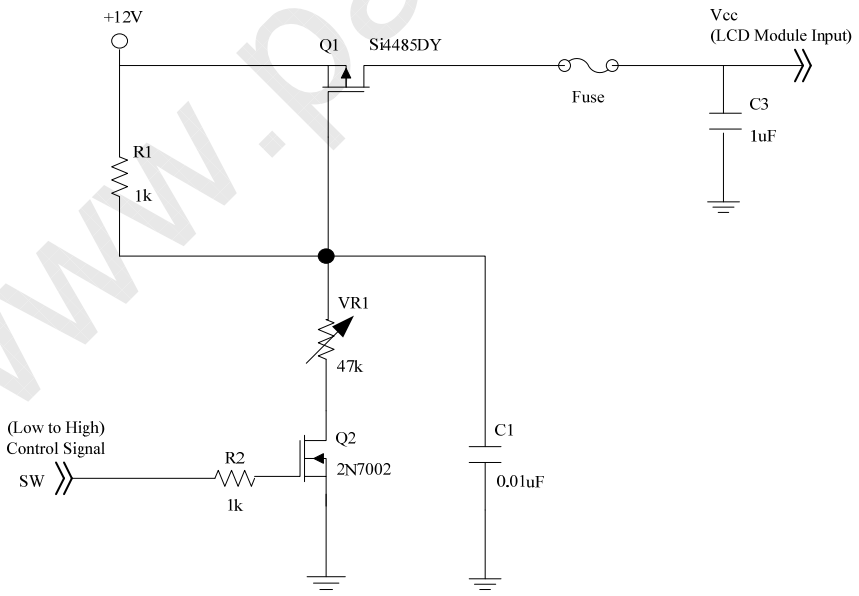
3.1 TFT LCD MODULE

(Ta = 25 ± 2 ºC)

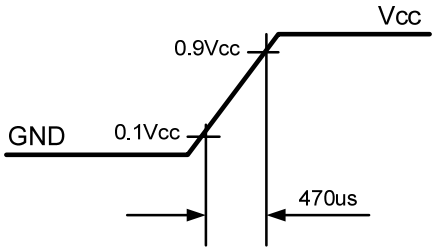
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCC	10.8	12	13.2	V	(1)
Power Supply Ripple Voltage		VRP	-	-	350	mV	
Rush Current		IRUSH	-	-	5.0	A	(2)
Power Supply Current	White Pattern	-	-	1.6	-	A	(3)
	Vertical Stripe	-	-	2.3	2.8	A	
	Black Pattern	-	-	1.6	-	A	
LVDS interface	Common Input Voltage	VLVC	1.125	1.25	1.375	V	
	Terminating Resistor	RT	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 °C, fv = 120 Hz, whereas a power dissipation check pattern below is displayed.

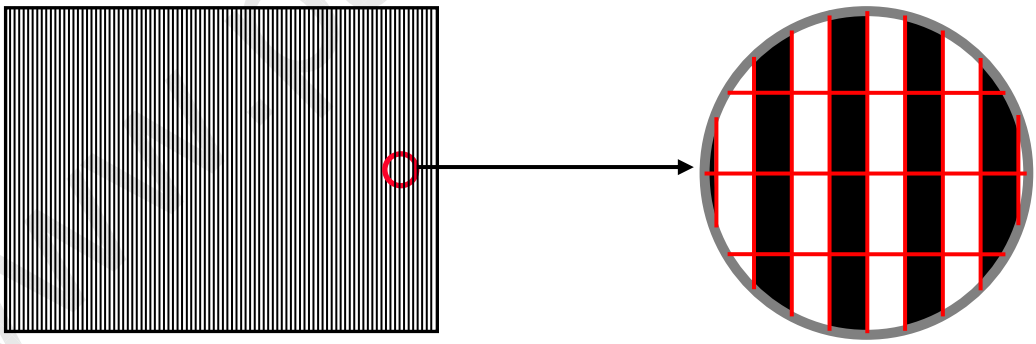
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



Active Area

3.2 BACKLIGHT UNIT

3.2.1 CCFL(Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta=25± 2 ºC)

(Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	VL	-	1175	-	VRMS	-
Lamp Current	IL	8.8	9.3	9.8	mARMS	(1)
Lamp Turn On Voltage	VS	-	-	1820	VRMS	Ta = 0 ºC
		-	-	1620	VRMS	Ta = 25 ºC
Operating Frequency	FL	40	-	70	KHz	
Lamp Life Time	LBL	50,000		-	Hrs	(2)

3.2.2 INVERTER CHARACTERISTICS

(Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P_{BL}	-	130	138	W	(5), IL =9.3mA
Power Supply Voltage	VBL	22.8	24.0	25.2	VDC	
Power Supply Current	IBL	-	5.4	-	A	Non Dimming
Input Ripple Noise	-	-	-	912	mVP-P	VBL=22.8V
Oscillating Frequency	FW	37	40	43	kHz	
Dimming Frequency	FB	150	160	170	Hz	
Minimum Duty Ratio	DMIN	-	20	-	%	

Note (1) Lamp current is measured by utilizing AC current probe.

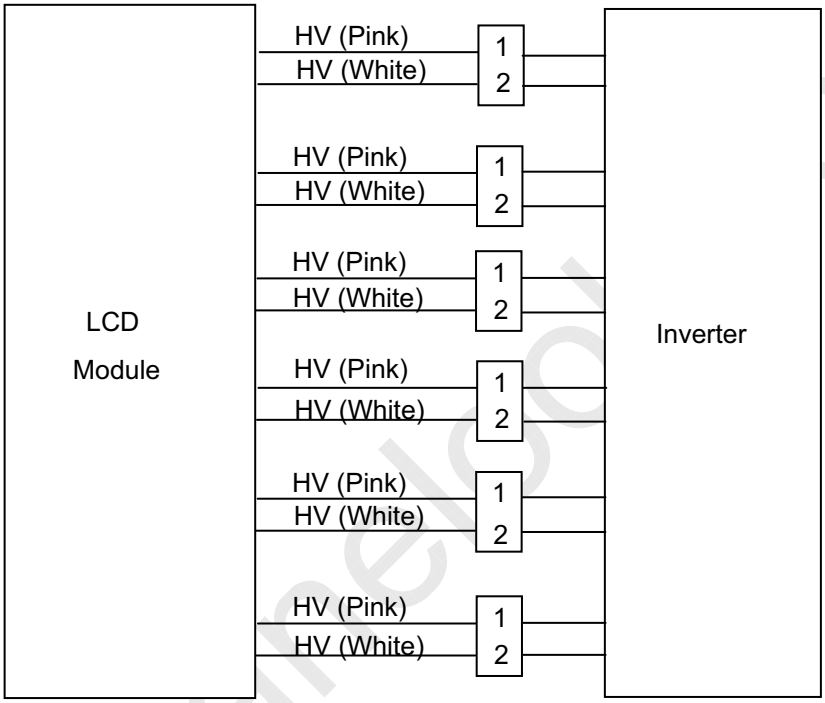
Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at

the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2℃ and I_L =9.0~ 9.6mArms.

Note (5) The measurement condition of Max. value is based on 47" backlight unit under input voltage 24V, average lamp current 9.6 mA and lighting 30 minutes later.



3.2.3 INVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	VIPWM	—	2.85	3.0	3.15	V	maximum duty ratio
	MIN		—	—	0	—	V	minimum duty ratio
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.0	V	Duty on
	LO		—	0	—	0.8	V	Duty off
Status Signal	HI	Status	—	3.0	3.3	3.6	V	Normal
	LO		—	0	—	0.8	V	Abnormal
VBL Rising Time		Tr1	—	30	—	—	ms	10%-90%V_{BL}
VBL Falling Time		Tf1	—	30	—	—	ms	
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
PWM Signal Rising Time		TPWMR	—	—	—	50	us	
PWM Signal Falling Time		TPWMF	—	—	—	50	us	
Input Impedance		Rin	—	1	—	—	MΩ	
PWM Delay Time		TPWM	—	100	—	—	ms	
BLON Delay Time		T_{on}	—	300	—	—	ms	
		T_{on1}	—	300	—	—	ms	
BLON Off Time		Toff	—	300	—	—	ms	

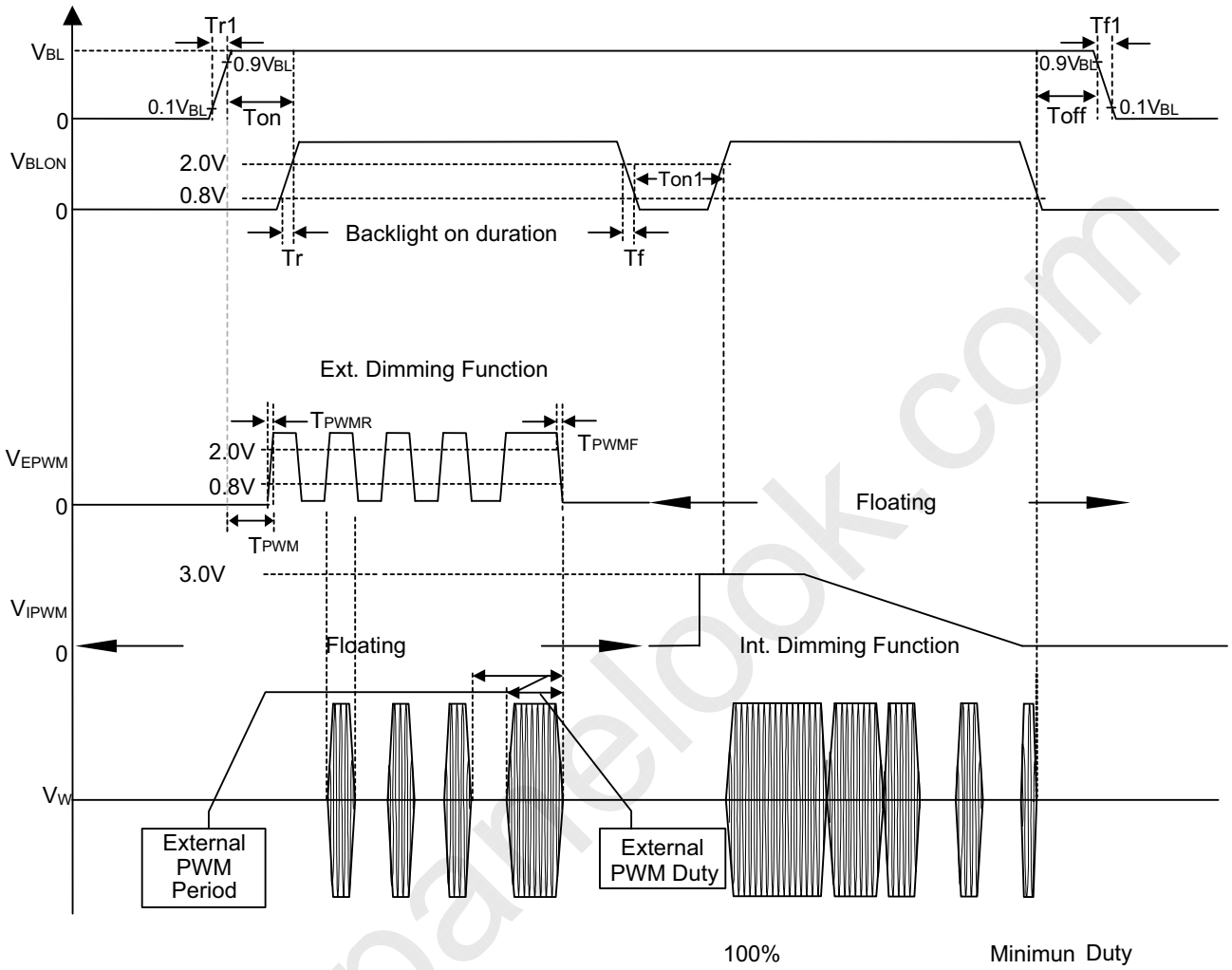
Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the following figure. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

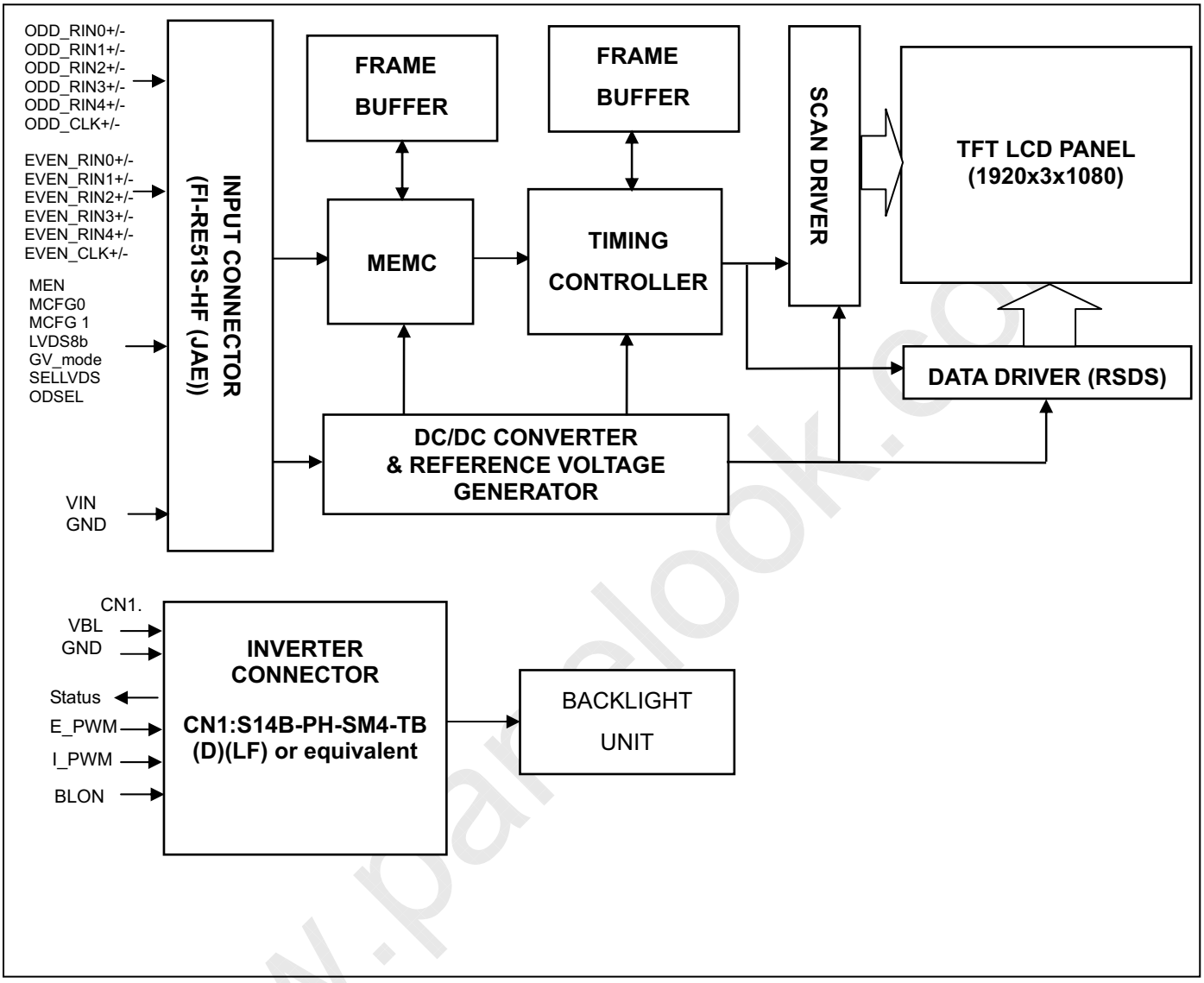
Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

CNF1 Connector Part No.: JAE Taiwan (台灣航空電子) FI-RE51S-HF or equal.

Pin	Name	Description	Note
1	GND	Ground	
2	MEN	MEMC function selection	4
3	MCFG0	MEMC function selection	4
4	MCFG1	MEMC function selection	4
5	LVDS8b	8bit/10bit LVDS input selection	5
6	GV_mode	Graphic / Video mode selection	6
7	SELLVDS	LVDS data format Selection	2
8	Res.	No Connection	
9	Res.	No Connection	
10	ODSEL	Overdrive Lookup Table Selection	3
11	GND	Ground	
12	ERX0-	2nd pixel Negative LVDS differential data input. Channel 0	
13	ERX0+	2nd pixel Positive LVDS differential data input. Channel 0	
14	ERX1-	2nd pixel Negative LVDS differential data input. Channel 1	
15	ERX1+	2nd pixel Positive LVDS differential data input. Channel 1	
16	ERX2-	2nd pixel Negative LVDS differential data input. Channel 2	
17	ERX2+	2nd pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	ECLK-	2nd pixel Negative LVDS differential clock input.	
20	ECLK+	2nd pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	ERX3-	2nd pixel Negative LVDS differential data input. Channel 3	
23	ERX3+	2nd pixel Positive LVDS differential data input. Channel 3	
24	ERX4-	2nd pixel Negative LVDS differential data input. Channel 4	
25	ERX4+	2nd pixel Positive LVDS differential data input. Channel 4	
26	N.C.	No Connection	1
27	N.C.	No Connection	1
28	ORX0-	1st pixel Negative LVDS differential data input. Channel 0	
29	ORX0+	1st pixel Positive LVDS differential data input. Channel 0	
30	ORX1-	1st pixel Negative LVDS differential data input. Channel 1	
31	ORX1+	1st pixel Positive LVDS differential data input. Channel 1	
32	ORX2-	1st pixel Negative LVDS differential data input. Channel 2	
33	ORX2+	1st pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	OCLK-	1st pixel Negative LVDS differential clock input.	
36	OCLK+	1st pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	ORX3-	1st pixel Negative LVDS differential data input. Channel 3	

39	ORX3+	1st pixel Positive LVDS differential data input. Channel 3	
40	ORX4-	1st pixel Negative LVDS differential data input. Channel 4	
41	ORX4+	1st pixel Positive LVDS differential data input. Channel 4	
42	N.C.	No Connection	1
43	DEMO	Demo window enable	7
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	1
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

Note (1) Reserved for internal use. Please leave it open.

Note (2)

SELLVDS	Mode
L(default)	VESA
H	JEIDA

L: Connect to GND, H: Connect to +3.3V

Note (3) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance with the frame rate to optimize image quality.

ODSEL	Description
L(default)	Lookup table was optimized for 60 Hz frame rate input.
H	Lookup table was optimized for 50 Hz frame rate input.

L: Connect to GND, H: Connect to +3.3V

Note (4) Motion Engine (ME) Level & Demo Function Table

Motion engine level must be adjusted after video mode is selected (or entered).

Adjusting the motion engine level in graphic mode has no effect

		MEN	MCFG1	MCFG0	Notes		
Blanking	**Blanking disable**	0	0	0	**(a)**		
	Auto blanking	0	0	1	**(b)**		
	Blanking enable	0	1	0	**(c)**		
				Effect of ME →	**De blur**	**De judder**	**Halo**
Demo mode (d)		0	1	1	Demo Window		
ME Level	**Strong**	1	0	0	Enable	Strong	Strong
	Medium(Default)	1	0	1	Enable	Normal	Normal
	Weak	1	1	0	Enable	×	×
	OFF	1	1	1	×	×	×
		(e) (f) (g)					

(a) Module re-starts processing video signals from Frontend scaler control board.

(b) During sync unstable period such as format change, 60Hz <-> 50Hz .
MCFG0 can be used to insert blanking of 500ms. This signal is toggled.

(c) Module continues to insert blanking until blanking disable signal is received from frontend scaler board.

(d) Demo window mode: Demo Window appears to the left half of display area. Left side with frame is 120Hz with MEMC, and right side is 120Hz w/o motion compensation.

(e) GPIO (General Purpose I/O) sequence of ME Level: (1) MEN; (2) MCFG1; (3) MCFG0.
GPIO sequence of Blanking Enable, Blanking Disable and Demo window: (1) MCFG1; (2) MCFG0; (3) MEN.

(f) Each scaler command must be maintained the same voltage level at least 100ms.

(g) 0 : Connect to GND, 1 : +3.3V

Note (5) 8bit/10bit LVDS input selection

LVDS8b	Bit depth
H(default)	8bit
L	10bit

L : Connect to GND, H : Connect to +3.3V

Note (6) Graphic / Video mode selection

There is no prohibited time period for switching between Graphic mode and Video mode.
When this switching signal is input, LCD will be reset and will re-start selected mode.

GV_mode	Mode select	MEMC ON/OFF
H(default)	Graphic mode	MEMC OFF
L	Video mode	MEMC ON

L : Connect to GND, H : Connect to +3.3V

Note (7) Demo window enable

Demo Window	
L(default)	**disable**
H	enable

L : Connect to GND, H : Connect to +3.3V

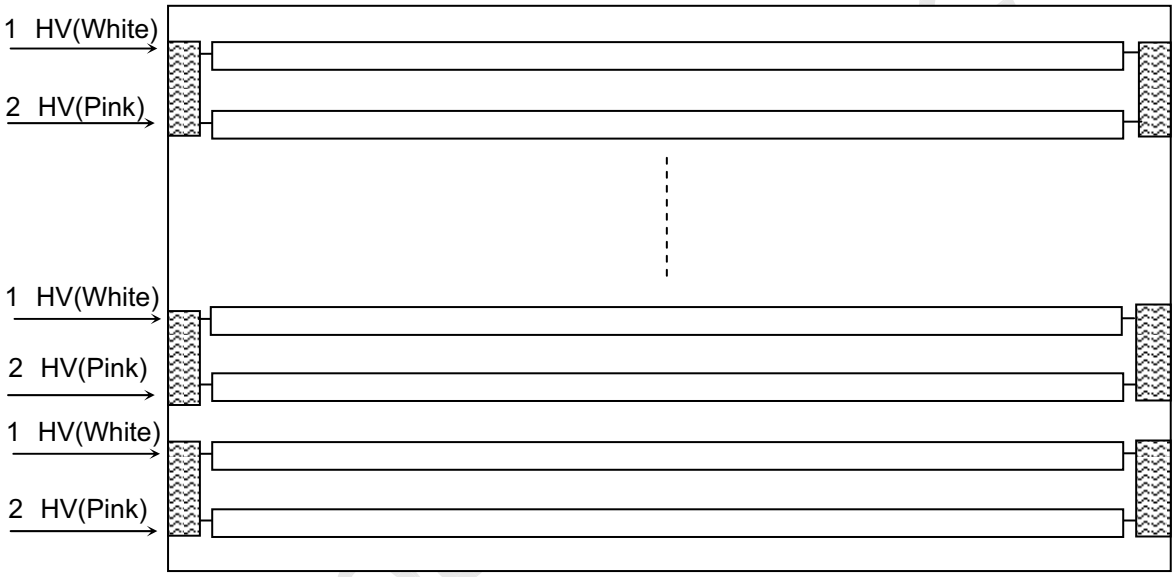
5.2 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

CN3~CN26: BHR-04VS-1 (JST).

Pin	Name	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BHR-04VS-1, manufactured by JST. The mating header on inverter part number is SM02(12.0)B-BHS-1-TB(LF).



5.3 INVERTER UNIT

CN1: S14B-PH-SM4-TB(D)(LF)(JST) or equivalent

Pin №	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	STATUS	Normal (3.3V) Abnormal(GND)
12	E_PWM	External PWM Control Signal
13	I_PWM	Internal PWM Control Signal
14	BLON	BL ON/OFF

Note (1) Pin 12: External PWM control (use pin 12): Pin 13 must open.

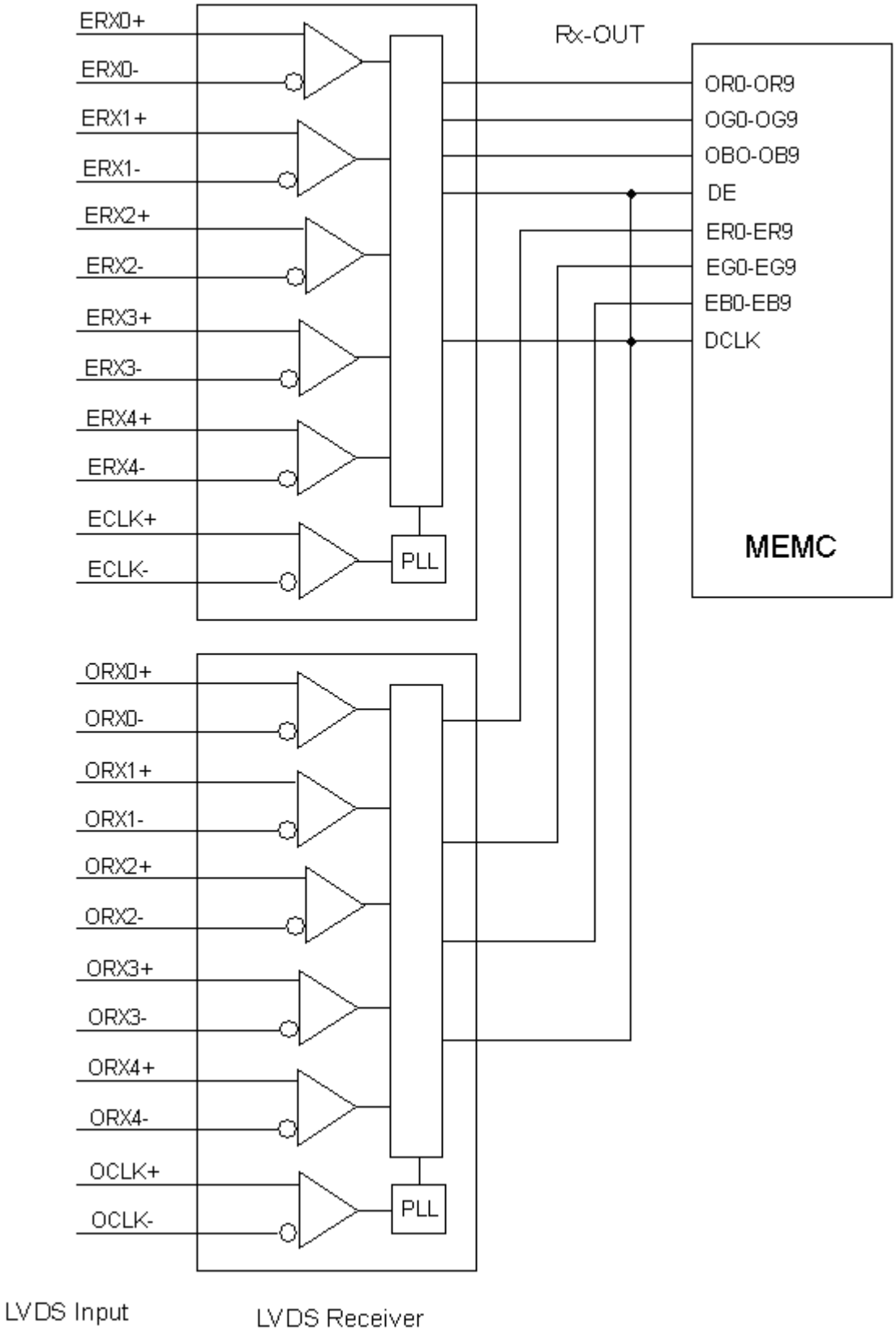
Note (2) Pin 13: Internal PWM control (use pin 13): Pin 12 must open.

Note (3) Pin 12 and Pin 13 can't open in the same period.

CN3~CN26: SM02(12.0)B-BHS-1-TB(LF)(JST) or equivalent

Pin №	Symbol	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

5.4 BLOCK DIAGRAM OF INTERFACE



AR0~AR9: First pixel R data

AG0~AG9: First pixel G data

AB0~AB9: First pixel B data

BR0~BR9: Second pixel R data

BG0~BG9: Second pixel G data

BB0~BB9: Second pixel B data

DE: Data enable signal

DCLK: Data clock signal

Notes (1) The system must have the transmitter to drive the module.

Notes (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

Notes (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

AR0~AR9: First pixel R data

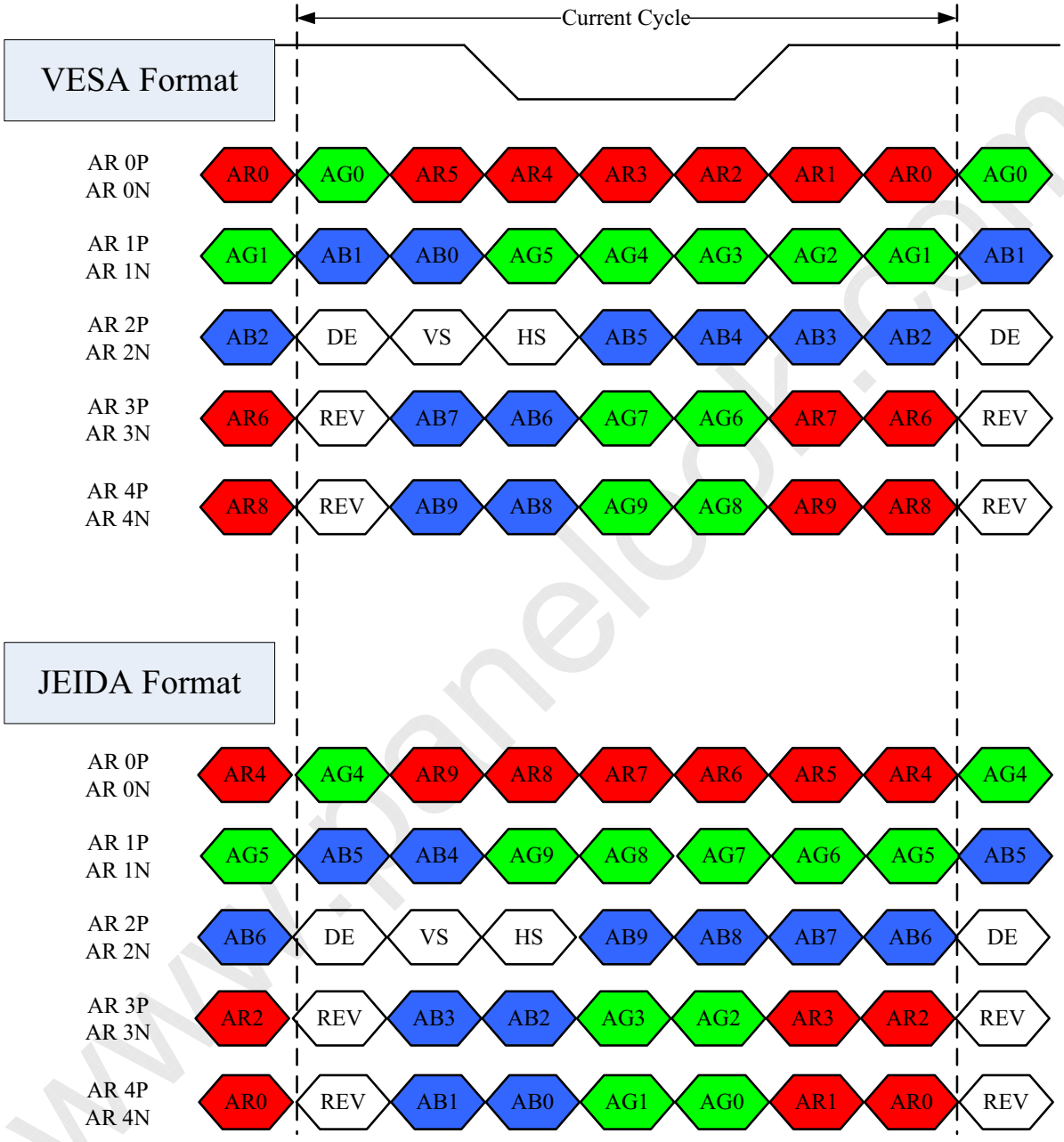
AG0~AG9: First pixel G data

AB0~AB9: First pixel B data

5.5 LVDS INTERFACE

VESA Format : SELLVDS = L or Open

JEIDA Format : SELLVDS = H



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSVD : Reserved

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

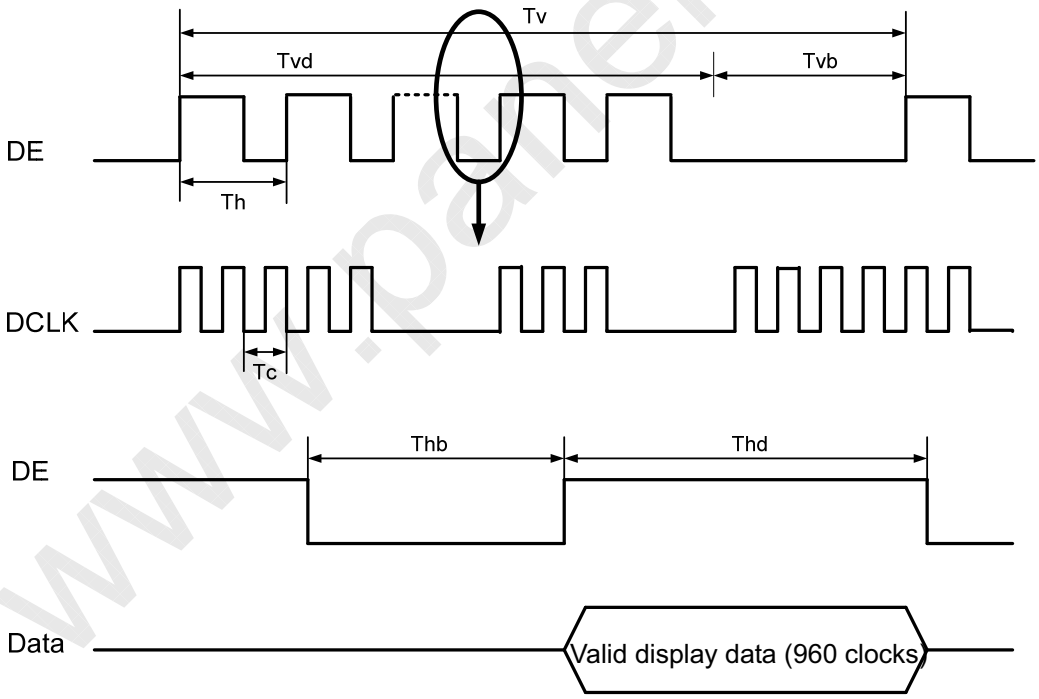
(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

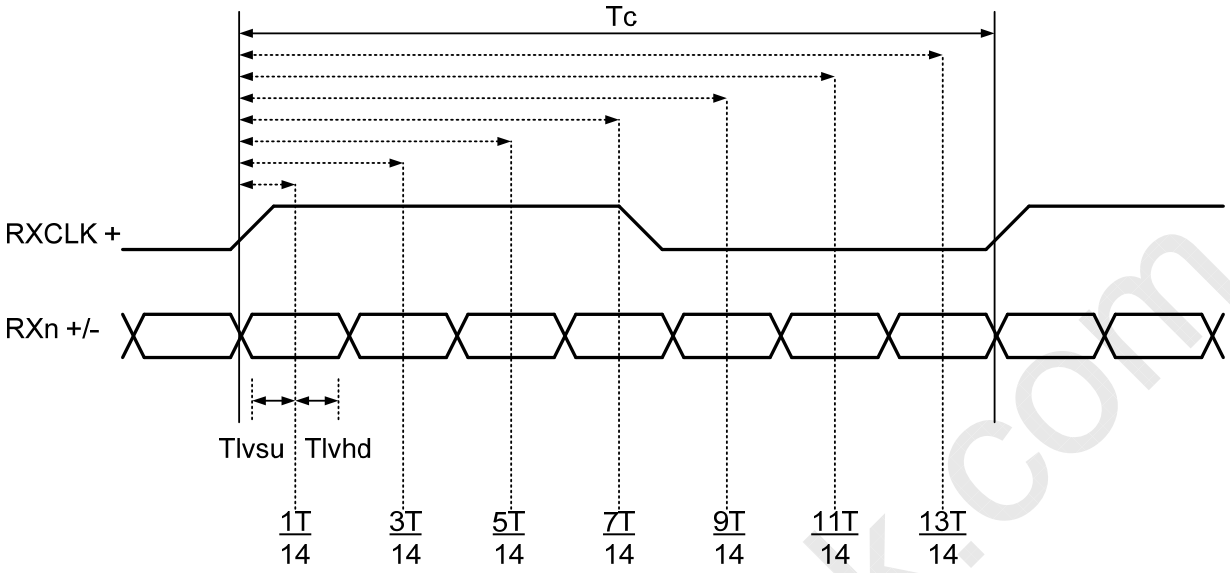
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74.25	78	MHz	-
	Input cycle to cycle jitter	Trcl	-	-	200	ps	-
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	-
	Hold Time	Tlvhd	600	-	-	ps	-
Vertical Active Display Term	Frame Rate		57	60	61	Hz	-
			47	50	53		
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	35	45	55	Th	-
Horizontal Active Display Term	Total	Th	1050	1100	1150	Tc	Th=Thd+Thb
	Display	Thd	960	960	960	Tc	-
	Blank	Thb	90	140	190	Tc	-

Note : Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

INPUT SIGNAL TIMING DIAGRAM



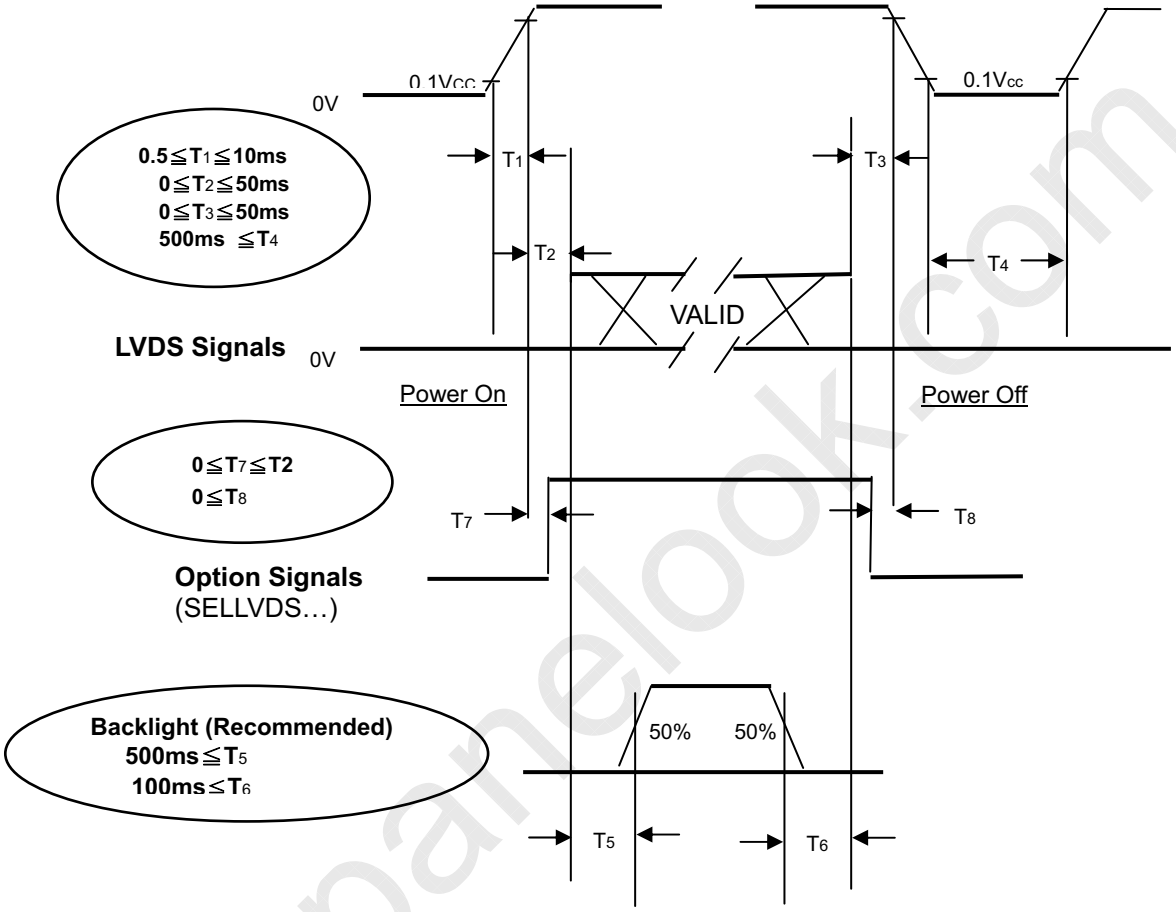
LVDS INPUT INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.



Power ON/OFF Sequence

Note.

(1) The supply voltage of the external system for the module input should follow the definition of Vcc.

(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance. If T2<0, that maybe cause electrical overstress failures.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

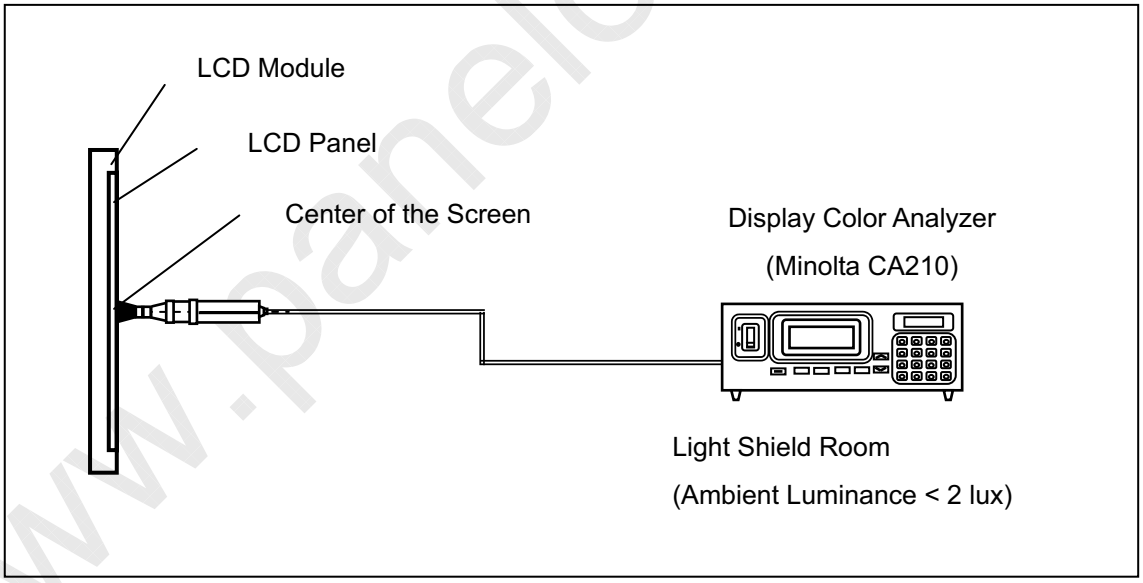
(5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	IL	9.3±0.5	mA
Oscillating Frequency (Inverter)	FW	40±3	KHz
Vertical Frame Rate	Fr	120	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



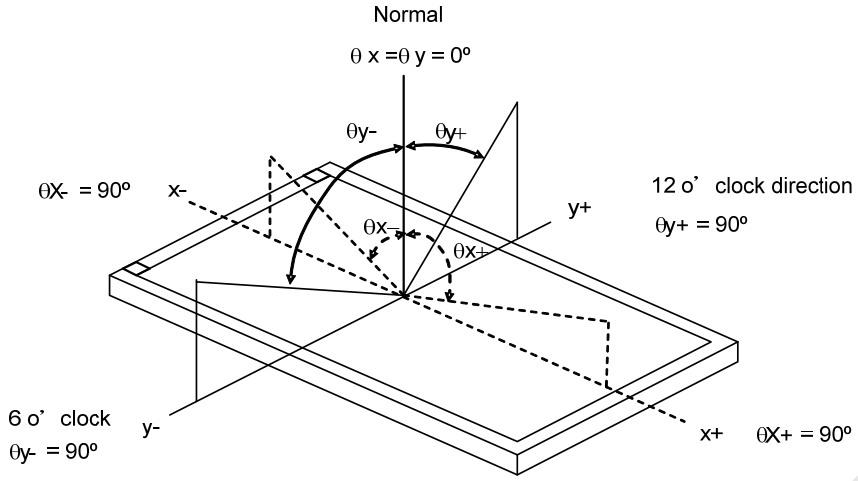
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0°, θy =0° Viewing angle at normal direction	3000	4000	-	-	Note (2)
Response Time		Gray to gray		-	4.5	9	ms	Note (3)
Center Luminance of White		LC		400	500	-	cd/m^2	Note (4)
White Variation		δW		-	-	1.3	-	Note (7)
Cross Talk		CT		-	-	4	%	Note (5)
Color Chromaticity	Red	Rx		Typ. -0.03	0.643	Typ. +0.03	-	-
		Ry			0.332		-	
	Green	Gx			0.272		-	
		Gy			0.599		-	
	Blue	Bx			0.152		-	
		By			0.067		-	
	White	Wx			0.285		-	
		Wy			0.293		-	
	Color Gamut	C.G		-	72	-	%	NTSC
Viewing Angle	Horizontal	θx+	CR≥20	80	88	-	Deg.	Note (1)
		θx-		80	88	-		
	Vertical	θY+		80	88	-		
		θY-		80	88	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Eldim EZ-Contrast 160R



Note (2) Definition of Contrast Ratio (CR):

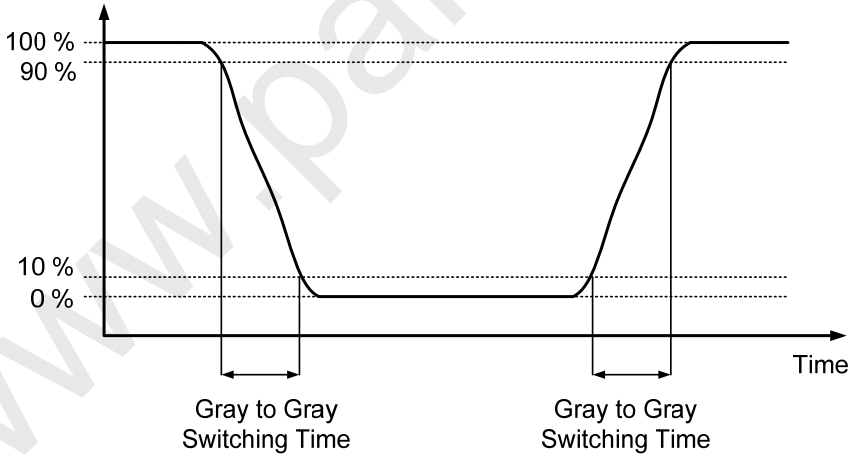
The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time:

Optical Response



The driving signal means the signal of gray level 0, 252, 508, 764, and 1023.Gray to gray average time means the average switching time of gray level 0, 252,508,764,1023 to each other.

Note (4) Definition of Luminance of White (LC, LAVE):

Measure the luminance of gray level 1023 at center point and 5 points

LC = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (6).

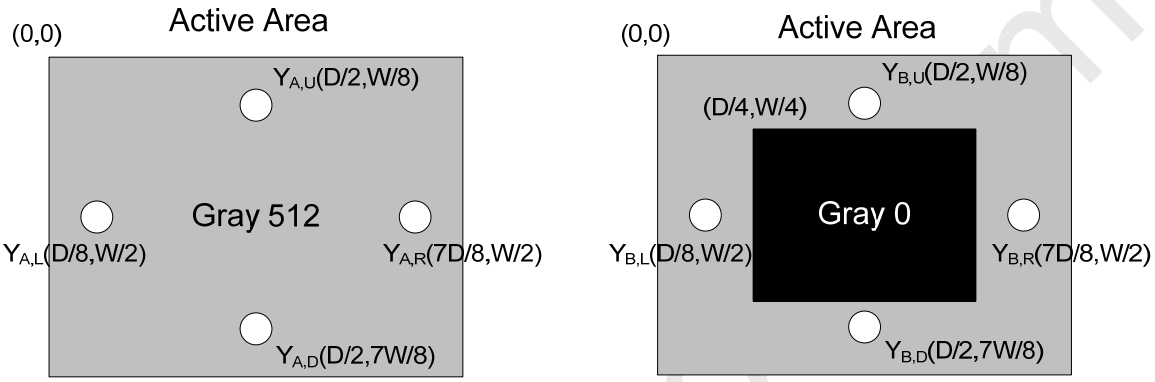
Note (5) Definition of Cross Talk (CT):

CT = | YB – YA | / YA × 100 (%)

Where:

YA = Luminance of measured location without gray level 0 pattern (cd/m2)

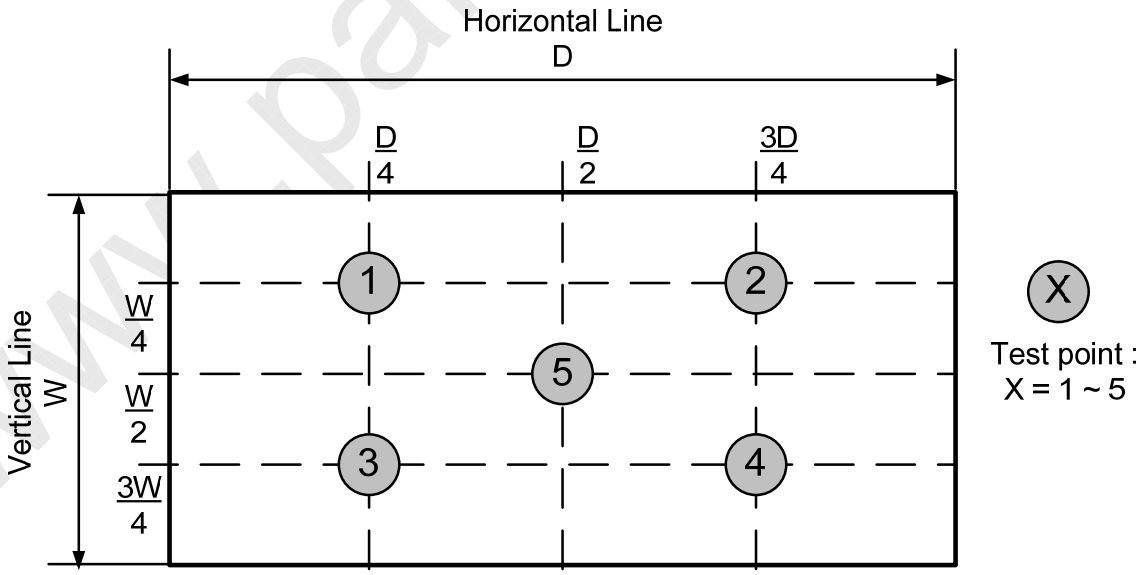
YB = Luminance of measured location with gray level 0 pattern (cd/m2)



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5] Do not plug in or pull out the I/F connector while the module is in operation.

[6] Do not disassemble the module.

[7] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[8] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[9] When storing modules as spares for a long time, the following precaution is necessary.

[9.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

[9.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[10] When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

[1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

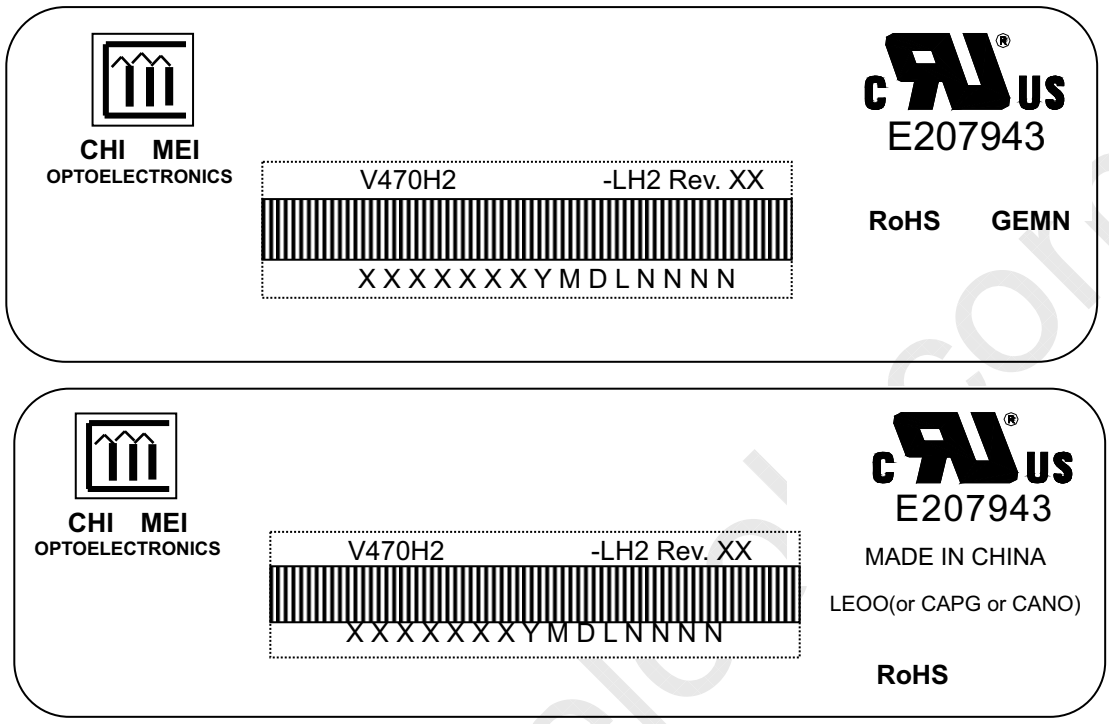
[2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[3] After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMO MODULE LABEL

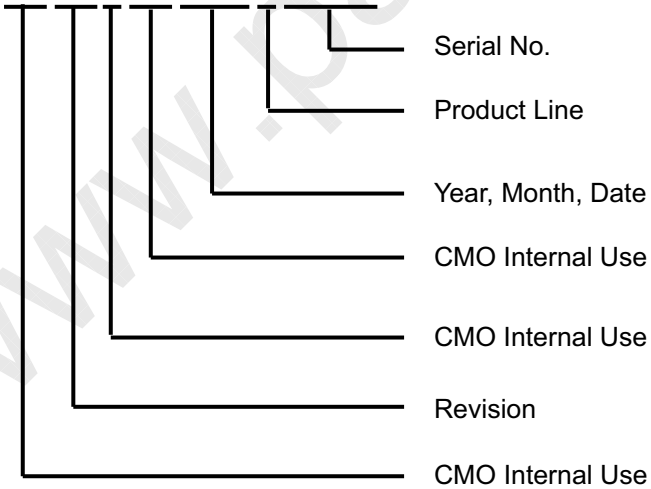
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V470H2-LH2

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year: 0~9, for 2000~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

Serial No.: Manufacturing sequence of product

Product Line: 1 -> Line1, 2 -> Line 2, …etc.

10. PACKAGING

10.1 PACKING SPECIFICATIONS

(1) 3 LCD TV modules / 1 Box

(2) Box dimensions : 1190(L)x280(W)x725(H)mm

(3) Weight : approximately 42 Kg (3 modules per box)

10.2 PACKING METHOD

Figures 10-1 and 10-2 are the packing method

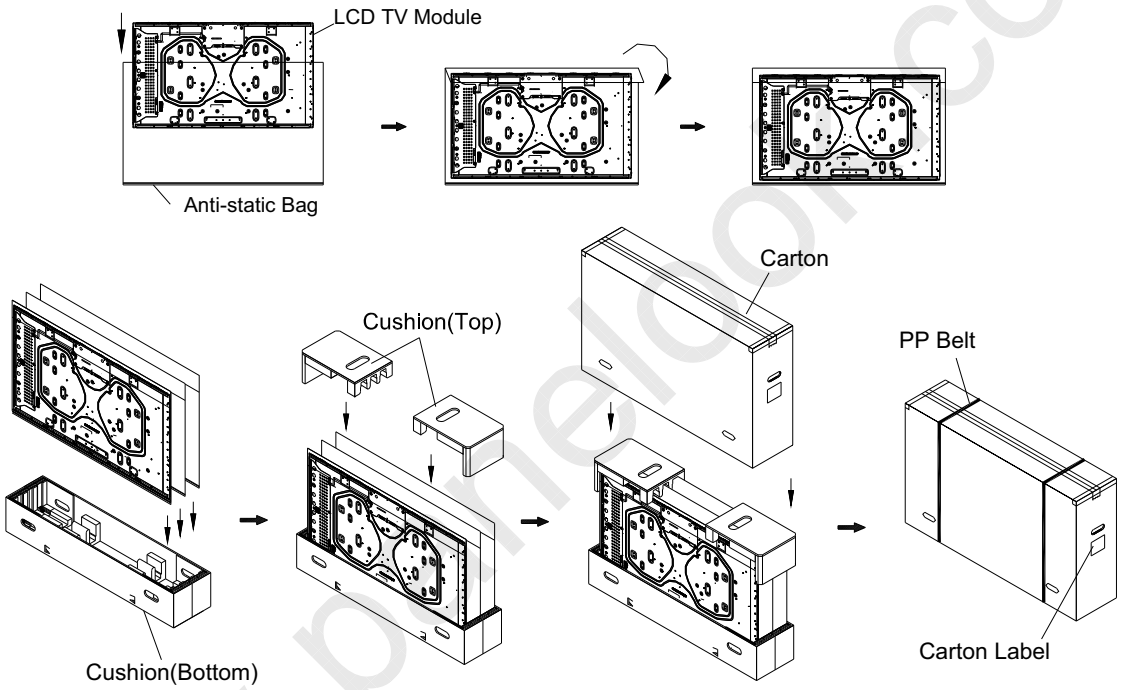
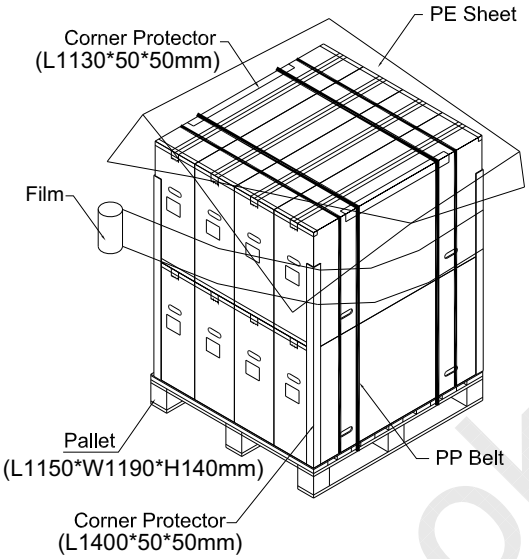


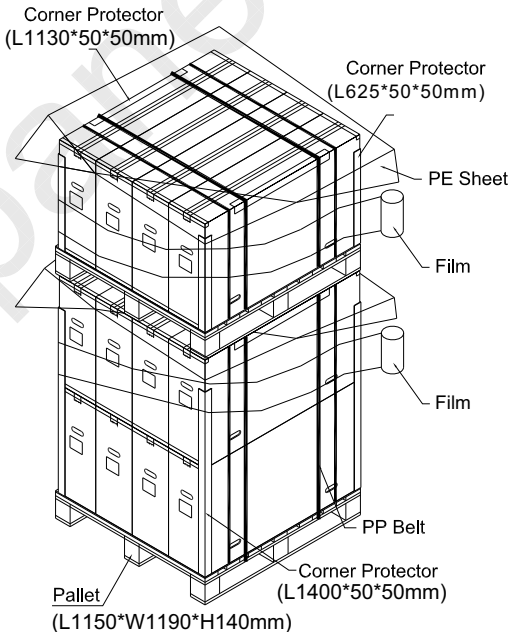
Figure.10-1 packing method

Air Transportation &

Sea / Land Transportation (40ft Container)



Sea / Land Transportation (40ft HQ Container)



Gross: 534kg

Figure.10-2 packing method

11. MECHANICAL CHARACTERISTICS